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INVESTIGATIONS OF GOLD SURFACE–STATE ENERGY LEVELS WHEN PRESENT AT A SILICON-SILICON DIOXIDE INTERFACE

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Gold diffusion into MOS device from the reverse of the silicon device substrate introduces two blocks of acceptor states close to the band edges. The logarithmic plot of resistivity against the reciprocal of the absolute temperature predicts the energy level position of these states: one at 0.13 eV from the conduction band edge and the other at 0.102 eV from the valence band edge.

The two deep normal bulk gold energy levels in silicon do not seem to be present at the oxidized silicon surface.

INTRODUCTION

Gold has been found to cause two deep-lying normal energy levels in the bulk silicon: one is donor energy level at 0.35 eV above the valence band edge and the other is acceptor energy level at 0.54 eV below the conduction band edge [1]. One of the practical applications of the introduction of gold into silicon devices is to control the minority carrier's lifetime and hence the device switching speed. Because of this practical application, the properties of gold in the bulk silicon have been studied extensively [2].

Interest in the near past has been centred on the effects of gold at the oxidized silicon surface because of the current importance of silicon planar technology. As a result, gold has been found to introduce negative surface charges at the Si–SiO_2 interface whatever the conductivity of the starting material, when diffused from the reverse of the MOS device substrate, thus allowing the possibility of controlling the threshold voltage of MOSFET and fabricating n-channel enhancement mode or p-channel depletion mode devices, particularly for complementary pair operation [3, 4].

It has been shown earlier [5] that the introduction of negative surface charges at the Si-SiO_2 interface by gold diffusion into oxidized silicon structure from the reverse of the device substrates is consistent with the introduction of two blocks of acceptor surface states by gold: one close to the valence band edge and the other near the conduction band edge. The physical location of these two blocks of acceptor surface states close to the respective band edges have been ascertained in eV units [6, 7] by using quasi-static capacitance voltage measurements by Gray and Brown's technique [8] and Hall effect measurements in gold-doped and undoped MOS devices.

In the present communication, the logarithmic plot of resistivity against the reciprocal of the absolute temperature is used to study the phenomenon with the aim of making a search for other energy levels, because the energy level positions in eV units can also be obtained from the slope of the linear portion of resistivity plotted logarithmically against the reciprocal of the absolute temperature.

EXPERIMENTAL RESULTS AND DISCUSSION

From the ratio of $C_{min.}/C_{max.}$ of a capacitance–voltage curve one can estimate the effective impurity doping concentration at the Si-SiO_2 interface and hence the resistivity. Tables 1 and 2 present some typical values of $C_{min.}/C_{max.}$, effective impurity doping concentration at the interface and the resistivity for p- and n-type gold-doped silicon devices with the initial resistivity of 2-6Ωcm and 1-2Ωcm respectively. Gold was diffused into MOS capacitors for 10 min. at 1000° in dry nitrogen gas and then a series of capacitance-voltage curves were measured at a signal frequency of 20 KHz from 293 to 77 K[6].

Fig. 1–2 demonstrate typical logarithmic plot of resistivity data against the reciprocal of the absolute temperature obtained from the p- and n-type gold-doped MOS capacitors. From the slope of the linear portion of the logarithmic plots of resistivity against the reciprocal of the absolute temperature, the energy positions of the

Table 1. Summary of measured $C_{min.}/C_{max.}$, the effective impurity doping concentration at the interface, and the resistivity as a function of absolute temperature (T), in p-type gold-doped MOS capacitor

$C_{min}/C_{max.}$	Doping level/cm^3 (impurity concentration)	Resistivity Ohm. cm)	$\frac{10^3}{T}$, K^{-1}
0.57	3×10^{15}	5	3.41
0.65	5×10^{15}	3	3.56
0.66	6×10^{15}	2.5	3.83
0.67	7×10^{15}	2.2	4.05
0.68	8×10^{15}	1.8	4.35
0.65	5×10^{15}	3.0	5.04
0.54	2×10^{15}	7.0	5.46
0.42	1×10^{15}	15.0	5.78
0.29	2×10^{14}	70.0	6.02
0.25	1.5×10^{14}	100.0	7.14
0.27	2×10^{14}	70.0	9.18
0.27	2×10^{14}	70.00	12.97

Table 2. Summary of measured $C_{min}/C_{max.}$, the effective impurity doping concentration at the interface, and the resistivity as a function of absolute temperature (T), in n-type gold-doped MOS capacitor

$C_{min}/C_{max.}$	Deoping level/cm^3 (impurity concentration).	Resistivity (Ohm.cm)	$\frac{10^3}{T}$, K^{-1}
0.49	1.5×10^{15}	3.0	3.41
0.45	1×10^{15}	4.80	3.56
0.44	9×10^{14}	5.25	3.88
0.42	8×10^{14}	6.00	4.13
0.41	7×10^{14}	7.00	4.39
0.40	6×10^{14}	8.00	4.72
0.39	5×10^{14}	9.50	5.04
0.38	4×10^{14}	12.00	9.62
0.37	4×10^{14}	12.00	12.90

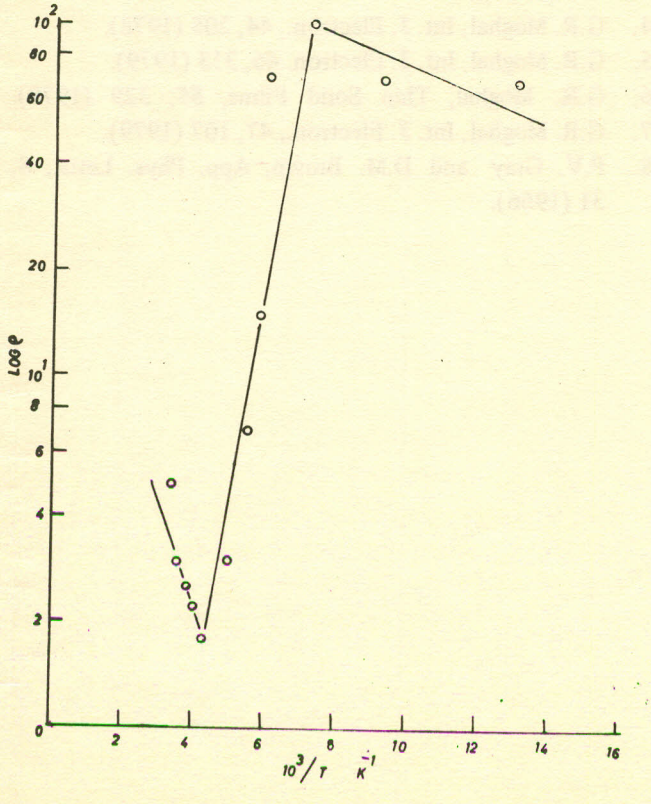

Fig. 1. Temperature-resistivity plot for gold-doped p-type silicon device.

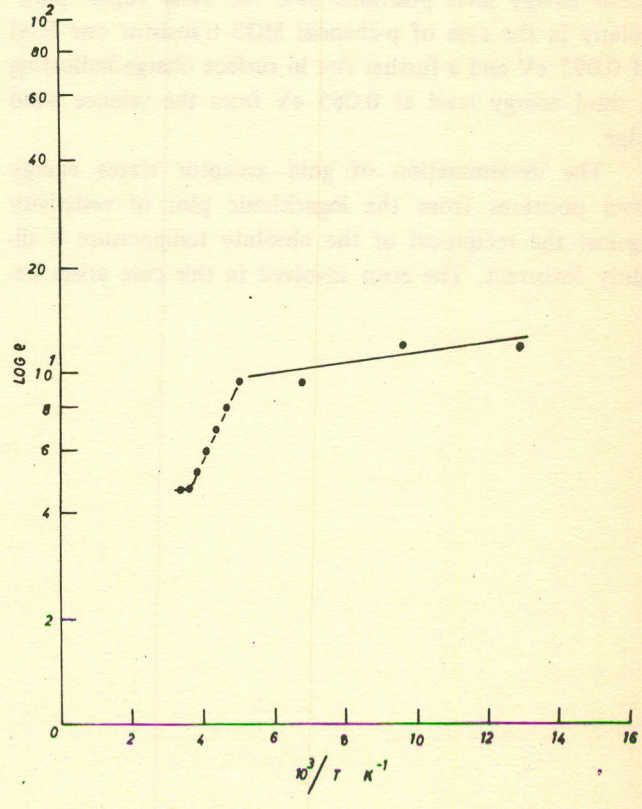

Fig. 2. Temperature-resistivity plot for gold-doped n-type silicon device.

gold acceptor states is 0.13 eV from the conduction band edge and 0.102 eV from the valence band edge. Since the silicon surface is already inverted, when the device measures the minimum values of the space charge capacitance and is separated from the bulk silicon by the depletion layer established around the inversion layer, it measures purely the surface effects of gold at the interface.

By analysing the measured series of capacitance - voltage curves from the gold-doped MOS capacitors as a function of temperature variations, using Gray and Brown's technique [8], we obtained the following energy positions of gold acceptor states: one at 0.13 eV from the conduction band edge and the other at 0.09 eV from the valence band edge [6].

The measurements of threshold voltage as a function of temperature variations in gold-doped p- and n-type MOS transistors leads us to the energy positions of the gold acceptor states: one at 0.12 eV from the conduction edge and a further rise in surface charge close to the valence band edge, suggesting another gold energy level near the band edge [7].

Hall effect measurements also confirm these acceptor states energy level positions near the band edges: particularly in the case of p-channel MOS transistor one level at 0.095 eV and a further rise in surface charge indicating a third energy level at 0.065 eV from the valence band edge.

The determination of gold acceptor states energy level positions from the logarithmic plot of resistivity against the reciprocal of the absolute temperature is slightly incorrect. The error involved in this case arises because the decrease of the mobility with temperature is somewhat greater than the increase of the density of states. However, the results obtained from these various separate experimental methods are in close agreement within the experimental error.

CONCLUSION

Gold introduces two blocks of acceptor surface states close to the band edges: one at 0.13 eV from the conduction band edge and the other at 0.102 eV from the valence band edge. These gold surface states energy levels at the oxidized silicon surface is the real cause of the positive shift of the MOS device characteristics along the gate voltage axis at room temperature irrespective of the conductivity of the starting material.

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