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CALCULATIONS AND CONTROLLING TECHNIQUES OF THEORETICAL THRESHOLD VOLTAGE FOR MOS TRANSISTORS

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By using the space charge neutrality condition in the vicinity of the gate insulator in the MOS structure, theoretical curves of the threshold voltages for both n- and p-channell MOS transistors are obtained as a function of substrate doping, inherent positive surface charge at the silicon–silicon dioxide interface and oxide thickness.

In addition some techniques of controlling the threshold voltage for MOS transistors with orienting crystal structure, multilayered gate structures and with the use of silicon gate and gold doping in the silicon substrates from the back side of the device are discussed.

INTRODUCTION

When a gate voltage is applied to the gate electrode of a MOS transistors with source shorted to the substrate, practically all of the applied voltage will be dropped across the insulating gate oxide approximately, because the resistivity of the insulator gate oxide is much greater than that of the semiconductor. It can easily be shown by Gauss's Law that a condition of macroscopic space charge neutrality must exist in the MOS structures consisting gate metallization, the insulating oxide and the semiconductor surface. By utilizing this space charge neutrality condition, the threshold voltage for both n- and p-channel MOSFET's can be evaluated. This communication will present the theoretical threshold voltage values for both n- and p-channel MOS transistors as a function of inherent positive surface charge present at the silicon – silicon dioxide interface, substrate doping, oxide thickness and work function considerations.

In addition, some methods of achieving low threshold voltage of the MOS field-effect transistors will be discussed.

The Space Charge Neutrality Condition for n-Channel Device

The charge distribution in an n-channel MOSFET is illustrated in Fig. 1. Fig. 1 (a) demonstrates the condition in which the gate voltage is too high to invert the surface of the p-type silicon substrate and form an n-channel. Fig. 1 (b) demonstrates the condition obtained at low gate voltages where only a depletion layer is present at the silicon surface. Q_g is the charge per unit area on the gate electrode. Q_{ss} is the inherent positive surface charge per unit area located at the silicon – silicon dioxide interface. Q_{inv} is the charge per unit area in the inversion layer and Q_{sd} is the charge per unit area in the depletion region. Presently the threshold voltage V_T, will be defined as the value of gate voltage for which the onset of inversion is observed. Initially at the onset of inversion layer the silicon surface is intrinsic, and the depletion region has not yet reached at its maximum depth. Thus, $Q_{inv} = 0$, and the condition for space charge neutrality is:

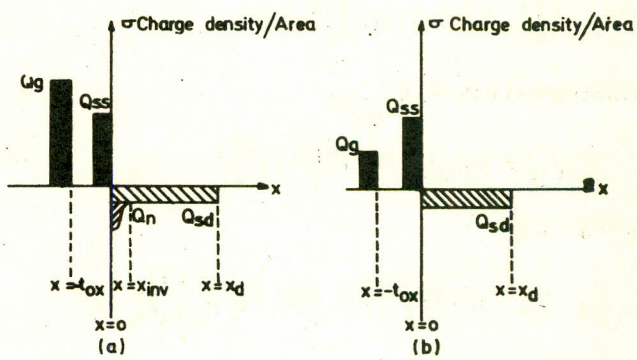

Fig. 1. Schematic diagram of charge distribution in an n-channel MOS field-effect transistor: (a) after inversion; (b) before inversion, ■ positive charge density; ▨ negative charge density.

$$Q_g + Q_{ss} + Q_{sd} = 0$$

Brotherton [1] has derived the relationship for the threshold voltage of the n-channel MOS field-effect transistor from the space charge neutrality equation and the charge neutrality equation and the charge per unit area in the dep-

letion region is approximately given by:

$$Q_{sd} = -qN_A X_d = -2qn_i L_D \left[2 \left(\text{Cosh} \left(\frac{q\psi_S}{kt} - \frac{q\psi_F}{kt}\right) - \text{Cosh} \frac{q\psi_F}{kt} + \frac{q\psi_S}{kt} \text{Sinh} \frac{q\psi_F}{kt} \right) \right]^{1/2} \quad (2)$$

when the silicon surface is intrinsic, $\psi_S = \psi_F$ and the charge per unit area in the depletion region is:

$$Q_{sd} \simeq -2qn_i L_D \left[2 \left(1 - \text{Cosh} \frac{q\psi_F}{kt} + \frac{q\psi_F}{kt} \text{Sin h} \frac{q\psi_F}{kt}\right) \right]^{1/2} \quad (3)$$

under conditions such that:

$$\frac{q\psi_F}{kt} > 1 \text{ and } \exp\left(\frac{q\psi_F}{kt}\right) \gg 1,$$

equation (3) reduces to:

$$Q_{sd} \simeq 2qn_i L_D \exp\left(\frac{q\psi_F}{2kt}\right)\left(\frac{q\psi_F}{kt} - 1\right) \quad (4)$$

substituting

$$N_A \simeq n_i \exp\left(\frac{q\psi_F}{kt}\right) \text{ and } L_D = \left[\frac{kT t_s}{2q^2 n_i}\right]^{1/2}$$

one obtains:

$$-Q_{sd} = \sqrt{\left[2qN_A t_s\left(\psi_F - \frac{kt}{q}\right)\right]} \quad (5)$$

The charge per unit area in the depletion region can be obtained as a function of the acceptor doping concentration provided the functional dependence of the Fermi potential with the bulk doping acceptor concentration is known. Using the relationship for the Fermi potential which includes the effect of the effective mass difference between bands as is shown in Fig. 2, the relationship between the charge per unit area in the depletion region and the acceptor doping concentration was calculated. The results are shown in Fig. 3.

The definition of threshold voltage used here differs from that of Grove [2] and Sah *et al.* [3] who define it as that value of gate voltage which is required to produce strong inversion. The charge on the gate per unit area can be written as:

$$Q_g = C_o V_o \quad (6)$$

Where C_o is the oxide capacitance per unit area and V_o is the voltage dropped across the oxide and

$$V_g = V_o + \phi_{ms} + \psi_s \quad (7)$$

Where ϕ_{ms} is the metal-semiconductor work function difference for the MOS structure as discussed by Lindmayer [4]. At the threshold voltage, $V_g = V_T$ and $\psi_S = \psi_F$.

Rearranging equation (1), (6) and (7) one obtains the following expression for the threshold voltage:

$$V_T = \frac{-Q_{sd}}{C_o} - \frac{-Q_{ss}}{C_o} + \phi_{ms} + \psi_F \quad (8)$$

Equation (8) gives an expression for the gate voltage, which is required to bring the silicon surface to the onset of inversion. If there were no surface traps present at the silicon – silicon dioxide interface, any additional gate voltage would attract conduction band electrons into the channel to form a conducting path between drain and source and hence the flow of current in the external circuit. The oxide capacitance per unit area is given by:

$$C_o = \frac{\epsilon_{ox}}{t_{ox}} \quad (9)$$

where ϵ_{ox} is the dielectric constant of the gate oxide and t_{ox} is the gate oxide thickness.

The Space Charge Neutrality Condition for p-Channel MOS Device

The charge distribution in a p-channel MOS field-effect transistor is illustrated in Fig. 2. It should be noted that the inversion layer charge density and the depletion layer charge density are positive quantities when the substrate material is n-type and are negative quantities when the substrate material is p-type.

p-Channel MOS field-effect transistors are usually fabricated on n-type substrates, the inversion and depletion layer charge densities will add to the inherent positive surface charge-density at the silicon – silicon dioxide interface. Therefore, the charge on the gate electrode will be negative as a result of the charge neutrality condition and hence the threshold voltage will be negative. For this reason, p-channel enhancement mode MOS transistors are easily made on both high - and low-resistivity substrates.

Figure 2 (a) illustrates the condition when the gate voltage is sufficiently negative to invert the surface of the n-type substrate and create a p-channel. Fig. 2 (b) illustrates the condition obtained at low negative gate voltages where only a depletion layer is present at the silicon surface. Once again, at the onset of inversion, $Q_{inv} = \theta$, and the condition for space charge neutrality is given by equation (1). The expression for the charge per unit area in the

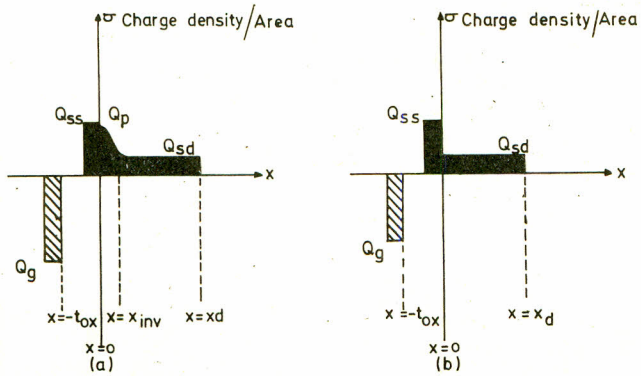

Fig. 2. Schematic diagram of charge distribution in a p-channel MOS field-effect transistor: (a) after inversion; (b) before inversion, ■ positive charge density; ▨ negative charge density.

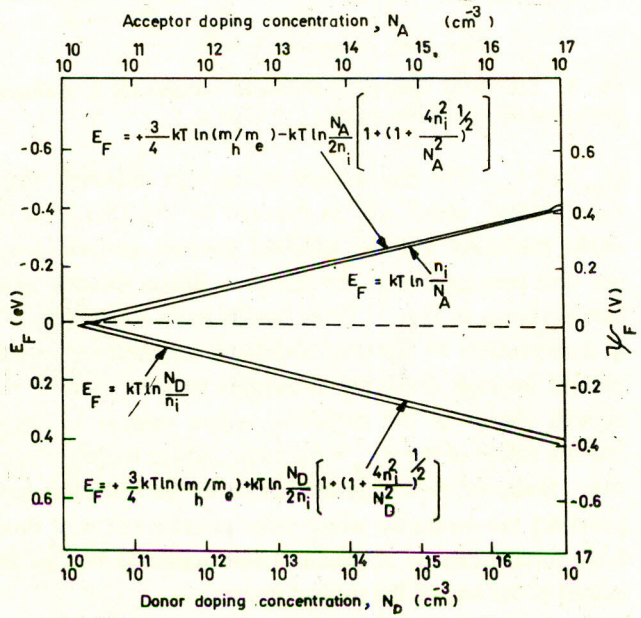

Fig. 3. Fermi potential as a function of impurity doping concentration.

depletion region can be obtained using a method similar to the one used for the case of the p-type substrate. The result, under conditions, such that:

$$\left(\frac{q\psi_F}{kT}\right) < -1 \text{ and } \exp\left(\frac{q\psi_F}{kT}\right) \ll 1,$$

can be given by:

$$Q_{sd} \simeq \sqrt{\left[-2qN_D\, t_s \left(\psi_F + \frac{kT}{q}\right)\right]} \qquad (10)$$

Since the Fermi potential is negative and usually much greater than (kT/q) for the n-type substrate, Q_{sd} will be positive. Using the relationship for the Fermi potential that includes the effect of the effective mass difference between bands, as shown in Fig. 3, the relationship between the charge per unit area in the depletion region and donor doping concentration was evaluated; the calculated results are shown in Fig. 4.

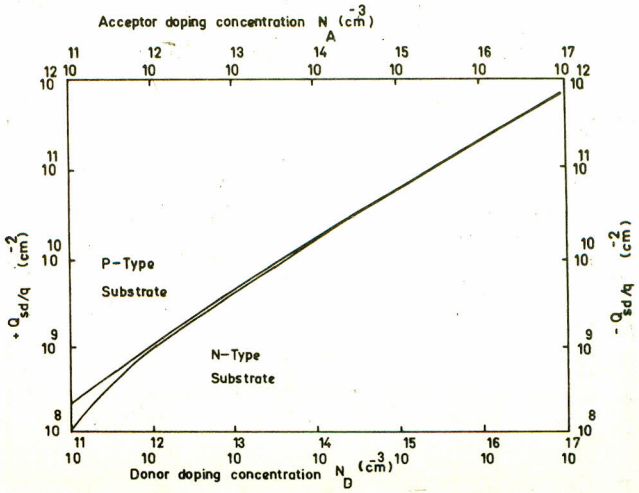

Fig. 4. The charge per unit area in the depletion region versus impurity doping concentration.

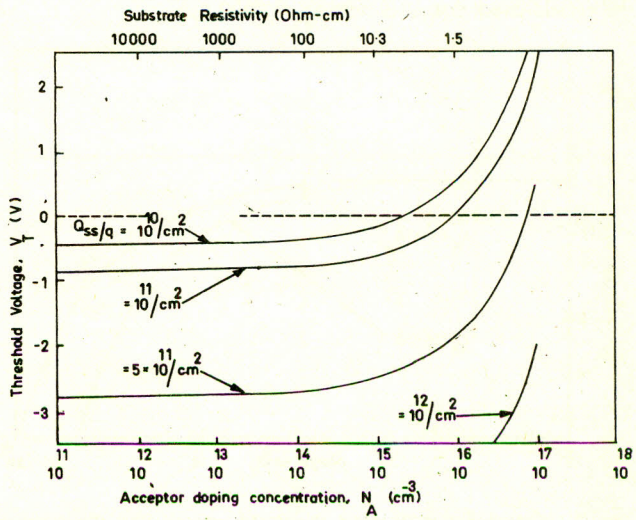

Fig. 5. Calculated theoretical threshold voltage for an n-channel MOS field-effect transistor with t_{ox} = 1000 Å.

The expression for the threshold voltage of the p-channel MOS field-effect transistor can easily shown to be:

$$V_T = \frac{-Q_{sd}}{C_o} - \frac{-Q_{ss}}{C_o} + \phi_{ms} + \psi_F \qquad (11)$$

Since $-Q_{sd}$ is a negative quantity, it adds directly with $-Q_{ss}$, making the threshold voltage for p-channel MOS field-effective transistors negative for all substrate resistivities.

Theoretical Curves of Threshold Voltages for n-Channel MOS Transistors

Using equation (8) and the values of Q_{sd} obtained from Fig. 4, the theoretical values of threshold voltages for n-channel MOS field-effect transistors were calculated as a function of the acceptor doping concentration in the

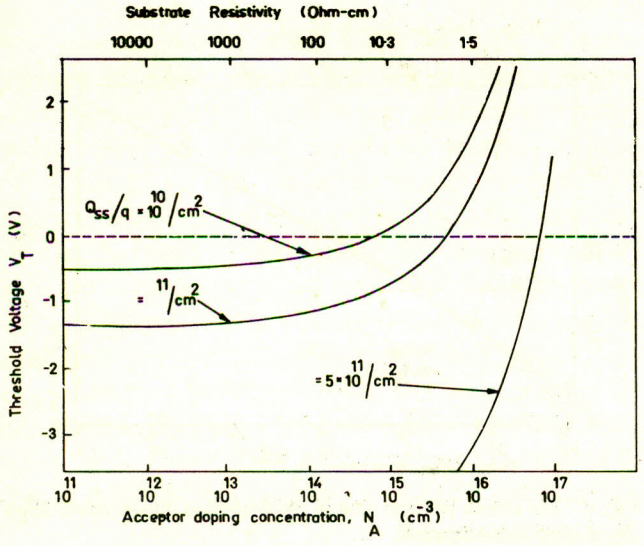

Fig. 6. Calculated theoretical threshold voltages for an n-channel MOS field-effect transistor with t_{ox} = 2000 Å.

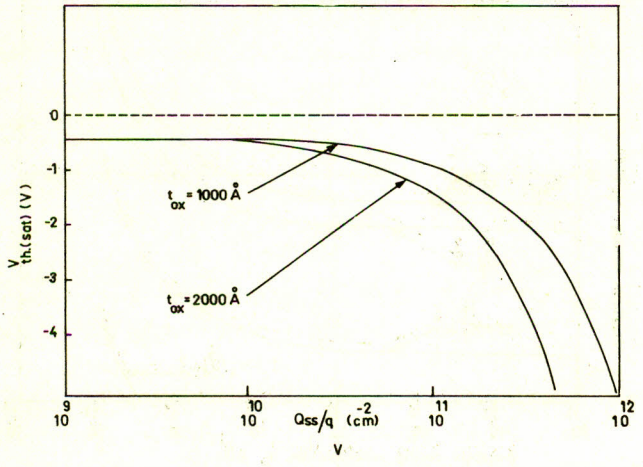

Fig. 7. Calculated theoretical threshold voltage Vth (Sat.) versus charge carriers Q_{ss}/q on high resistivity.

p-type substrate. The values of Q_{ss} and t_{ox} were varied as parameters. As a result, theoretical curves for the threshold voltages of n-channel MOS field-effect transistors are shown in Figs. 5 and 6. The well-known fact that it is more difficult to fabricate an enhancement unit if the amount of inherent + ve surface charge per unit area at the silicon – silicon dioxide interface is large and easily can be seen from these curves. For high substrate resistivites and low values of Q_{ss}, the threshold voltage is primarily determined by the $\theta_{ms} + \psi_F$ terms, and the value will be slightly negative (since the term is assumed to be –0.4V). For very low values of Q_{ss} and low resistivity substrates, the threshold voltage will be primarily determined by the charge per unit area in the depletion region, and enhancement unit may be easily made. For high substrate resistivities, the effect of the charge in the depletion region will be negligible, and the threshold voltage will saturate as a function of the doping concentration and will only vary with

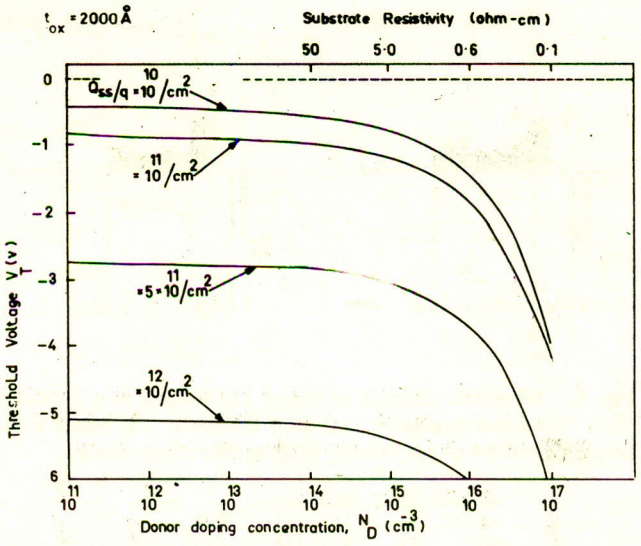

Fig. 8. Calculated theoretical threshold voltages for a p-channel MOS field-effect transistor with t_{ox} = 1000 Å.

Q_{ss} and t_{ox}. The dependence of the high resistivity threshold voltage, which will be denoted by Vth (Sat.), on the oxide thickness and the inherent positive surface charge per unit area located at the silicon – silicon dioxide interface is shown in Fig. 7. These results seem to indicate that it is impossible to fabricate n-channel enhancement mode-devices on high resistivity substrates because there is not enough charge in the depletion region present to cancel out the effect of the $\phi_{ms} + \psi_F$ term, which is always negative. However, recent developments in the discipline have provided the means by which more positive values of threshold voltage can be achieved. Those methods will be discussed at the end of the subject matter.

Theoretical Curves of Threshold Voltages for p-Channel MOS Transistors

Using equation (11) and the values of Q_{sd} obtained from Fig. 4, the theoretical values of threshold voltages for p-channel MOS field-effect transistors were calculated as a function of the bulk donor concentration in the n-type substrate. The values of Q_{ss} and t_{ox} were again varied as parameters. The resulting theoretical curves for the threshold voltages of p-channel MOS field effect transistors are shown in Figs. 8 and 9.

The behaviour of the p-channel MOS field-effect transistor's threshold voltage with substrate resistivity is very similar to the case of the n-channel MOS field effect transistor.

For low values of Q_{ss}, the threshold voltage is primarily determined by the $\phi_{ms} + \psi_F$ term, for high-resistivity substrates, and is primarily determined by the charge per unit area in the depletion region for low-resistivity substrates. In all cases the devices will operate only in the en-

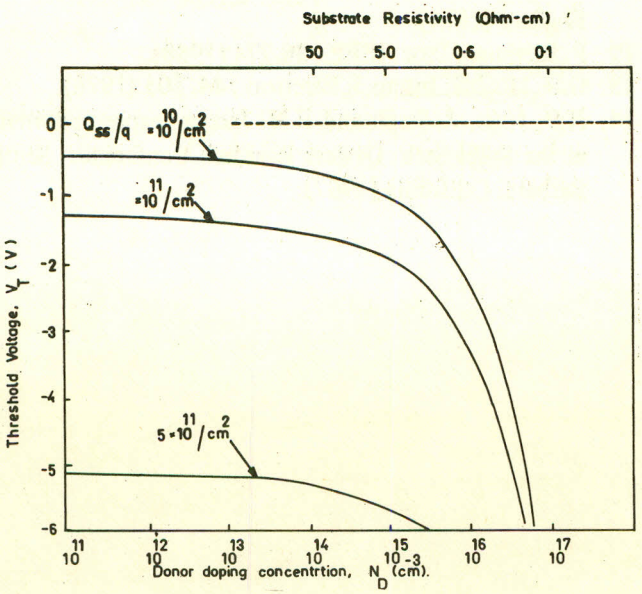

Fig. 9. Calculated theoretical threshold voltages for a p-channel MOS field-effect transistor with t_{ox} = 2000 A.

hancement mode. The threshold voltages will be more negative for lower-resistivity substrates when all other parameters are held constant. Since the charge in the depletion region will be negligible for high-resistivity substrates, it can easily be shown that the dependence of the high resistivity threshold voltage for p-channel MOS field-effect transistors will be exactly the same as that for n-channel MOS field-effect transistors (cf. Fig. 7).

Methods of Achieving Low Threshold Voltage

Thermally oxidized silicon is characterized by the presence of positive charges contained in the oxide itself and in ionized donor surface states [5, 6]. This leads to a shift of MOS field-effect transistors threshold voltage towards negative gate biases. It has been realized that this surface charge can be compensated for by diffusing gold into the back side of the silicon substrate [7 – 11]. The gold introduces negative charge centres at the silicon – silicon dioxide interface, thus allowing the possibility of controlling the threshold voltage of MOS field-effect transistors and of fabricating n-channel enhancement mode or p-channel depletion mode devices; particularly for complementary pair operation [12, 13].

By properly orienting the crystal structure in the semiconductor, the threshold voltage is reduced because the surface-state charge is less along the (100) plane than along the (111) plane.

Aluminium oxide and silicon dioxide are normally used in the double-insulator structure. The layer of SiO_2 is in direct contact with the silicon surface while the Al_2O_3 lies directly over the SiO_2. Silicon nitride is also oftenly used in place of silicon oxide as the insulating layer between the gate and the channel. Since the threshold voltage is inversely proportional to the gate capacitance; nitride increases capacitance because its dielectric constant is twice that of the oxide. The use of the double-insulator structure has been observed to shift the threshold voltage of MOS field-effect transistors by some + 1.2 to + 2.0 Volts from the values observed on similar devices with equivalent thickness of SiO_2 only [14].

Finally, the polycrystalline silicon gate instead of aluminium metal gate can be employed for obtaining the low threshold voltage for MOS field-effect transistors. Silicon gates are made of p-type polycrystalline silicon, whose work function is less than that of the aluminium used in ordinary MOS circuits. The difference between the work functions of the gate and the semiconductor, therefore, is less, and this influences the threshold voltage both directly and through a reduced surface state charge.

Moreover, polycrystalline silicon gate offer two advantages in fabrication; automatic gate alignment, and the possibility of mixing both bipolar and MOS circuits on the same substrate, without the n+ barrier diffusion.

Conclusion

Theoretical curves of threshold voltage versus substrate doping concentrations have been presented for both p- and n-channel MOS transistors as a function of oxide thickness and inherent positive surface charge density at the silicon – silicon dioxide interface. The conditions under which enhancement and depletion mode transistors can be fabricated have been discussed and related to MOS structures using gate insulators consisting of sandwiches of SiO_2 and Al_2O_3; SiO_2 and silicon nitride, polycrystalline silicon gate and gold doping in the substrates from the backside of the device.

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